IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
Deshpande et al.

Serial No.: 10/709,048

Filed: April 8, 2004

Group Art Unit: 2814

Examiner: Ingham, John C.

Atty. Docket No.: FIS920030397US1

For: A MANUFACTURABLE METHOD AND STRUCTURE FOR DOUBLE SPACER CMOS WITH OPTIMIZED NFET/PFET PERFORMANCE

Commissioner of Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. §1.131

We, the inventors of the invention defined by claims 1-2, 4-9, 12-14, 26-29 of U.S. Patent Application Serial No. 10/709,048 hereby declare the following:

[0001] The purpose of this declaration is to prove that we conceived the claimed invention prior to the earliest effective prior art date of U.S. Patent No. 7,064,396 to Chen which is presently understood to be March 1, 2004. The following shows that we conceived our invention prior to March 1, 2004 and that we were diligent from our date of conception to its reduction to practice and were further diligent to the date of the filing of our patent application, which has a filing date of April 8, 2004 (hereinafter referred to as the "Patent Application").

[0002] We are all the inventors of the subject matter claimed in claims 1-2, 4-9, 12-14, 26-29 of U.S. Patent Application Serial No. 10/709,048.

[0003] During all time periods mentioned herein, and specifically between our conception date and the filing date of the application, all activities described herein occurred in the United States.

[0004] Proof of the conception of the claimed invention prior to March 1, 2004, and diligence in reducing the invention to practice and filing the Patent Application is demonstrated in the attached Exhibit, labeled as Exhibit A.

[0005] As shown in Exhibit A, which is an invention disclosure form typically used by the designated Assignee, International Business Machines Corporation, we conceived the claimed invention at a date prior to March 1, 2004. As permitted by MPEP §715.07, the dates on Exhibit A have been removed; however, we hereby declare that all dates corresponding to the conception date and reduction to practice occurred prior to March 1, 2004. Further, the invention was actually conceived before Exhibit A was prepared. Therefore, our conception date actually predates Exhibit A.

[0006] Exhibit A specifically discloses the claimed invention as defined by the independent claims. For example, independent claim 1 defines an integrated circuit structure comprising: a substrate; first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors; second-type

transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors; first silicide regions proximate said first spacers of said first-type transistors; and second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors. Independent claim 8 defines an integrated circuit structure comprising: a substrate; first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors; second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors; first-type impurity implants in areas of said substrate completely outside of said first spacers of said first gate conductors; second-type impurity implants in areas of said substrate completely outside of said second spacers of said second gate conductors; first silicide regions proximate said first spacers of said first-type transistors; and second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors. Independent claim 26 defines an integrated circuit structure comprising: a substrate; first-type transistors on said substrate, wherein said first-type transistors comprise first

gate conductors and first spacers adjacent said first gate conductors; second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors, and wherein said second spacers are only proximate said first spacers that are adjacent said second gate conductors and said second spacers are not proximate said first spacers that are adjacent said first gate conductors; first-type impurity implants in areas of said substrate completely outside of said first spacers of said first gate conductors; second-type impurity implants in areas of said substrate completely outside of said second spacers of said second gate conductors; first silicide regions proximate said first spacers of said first-type transistors; and second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors.

[0007] Exhibit A clearly describes the above features. In fact, the descriptions provided in Exhibit A served as the basis for the specification, drawings, and claims of the Patent Application. The features provided in dependent claims 2, 4-7, 9, 12-14, 27-29 are generally inferred in Exhibit A.

[0008] We were diligent from the date of conception in reducing the invention to practice and in pursuing, preparing, and filing the Patent Application. More specifically, on April 23,

2003, information similar to that shown in Exhibit A were presented to a patent attorney to determine whether a patent application should be prepared.

[0009] On November 14, 2003, a patent attorney was instructed to prepare a patent application that eventually became the Patent Application. The Patent Application was eventually prepared and filed on April 8, 2004.

[0010] The foregoing declarations are made according to our best recollection upon review of the appropriate documents and notes, and I hereby acknowledge that willful false statements and the like are punishable by fine or imprisonment, or both (18 USC §1001) and may jeopardize the validity of the application or any patent issuing thereon. All statements made herein are made of our own knowledge and are true and all statements that are made on information and belief are believed to be true.

[SIGNATURE PAGES FOLLOW]

Dominic J. Schepis — Date: 1/18/07

Sadanand V. Deshpande — Date

Brian L. Tessier — Date

Dominic J. Schepis — Date

Sadanand V. Deshpande — Date 01|18|2007

Brian L. Tessier — Date

Dominic J. Schepis — Date

Sadanand V. Desbpande — Date

Brian L. Tessier — Date 1/18/07

EXHIBIT A

Main Idea for Disclosure FIS8-2003-0213

Prepared for and/or by an IBM Attorney - IBM Confidential

Archived On [redacted]01:01:52 AM

Title of disclosure (in English)

A Manufacturable Method and Structure for Double Spacer CMOS with Optimized NFET/PFET Performance

Main idea of disclosure

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.

The optimization of high performance CMOS consists of getting the highest performance from both the NFET and PFET devices. Often, as observed in CMOS 10S, the best process for one device may cause lower performance in the other device. The NFET and PFET were found to each be optimum with a different sidewall spacer process. Unfortunately, the processes involved in building two different spacers on two different devices is challenging. Our disclosure provides a manufacturable way of optimizing the sidewalls on NFET and PFET devices separately, leading to the highest performance CMOS.

2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.

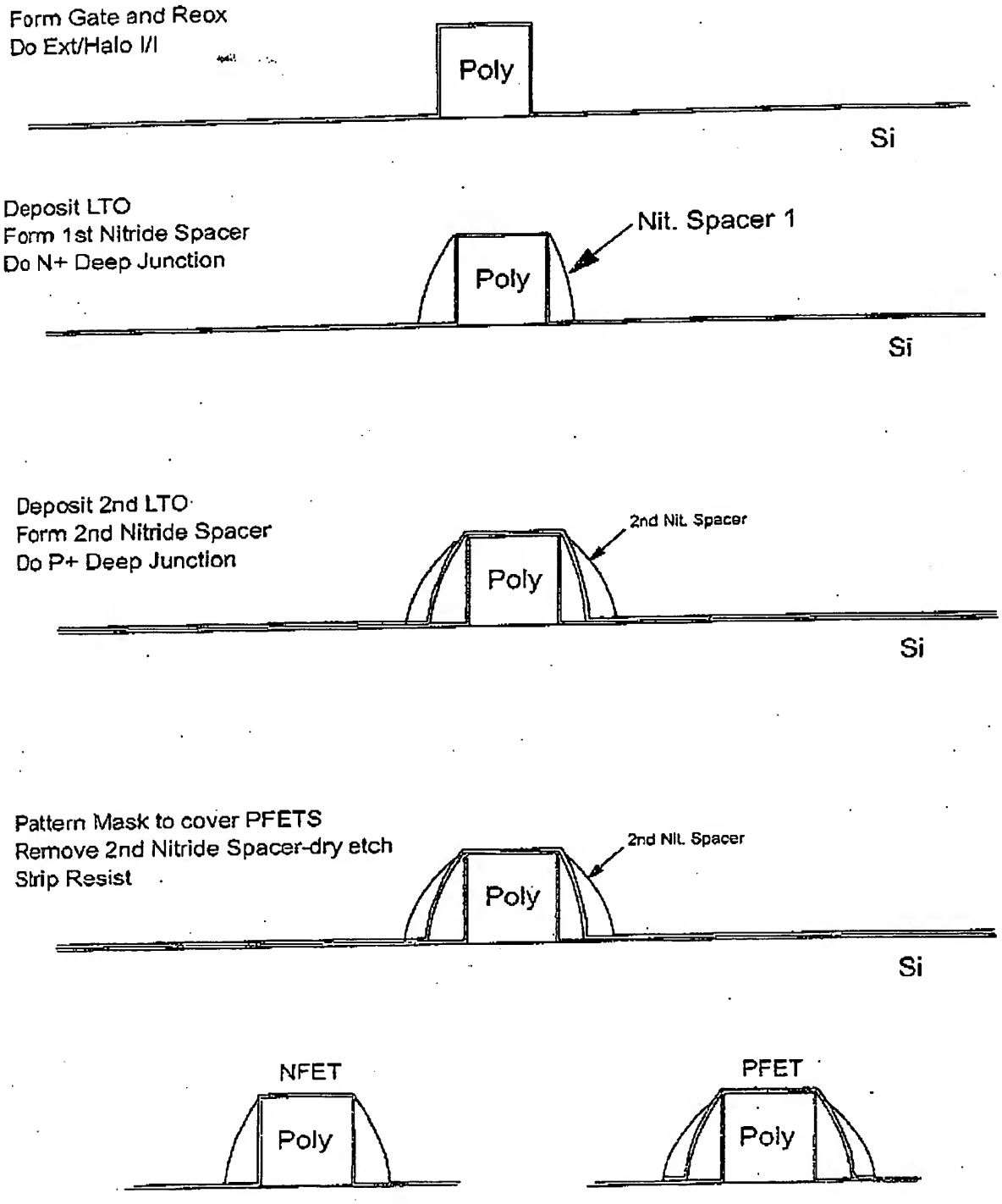
Our invention takes advantage of the known double spacer technique combined with a dry etching technique and sequence which leads to a dual spacer (I-shaped) result. The dual spacer methodology currently disclosed uses either a wet etch process which is less manufactuarble, or a dry approach which is difficult to perform due to the removal of a wide oxide spacer.

3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.

The invention works by creating different spacers on both the NFET and PFET devices. A method that is previously known is called double spacer, where a narrow spacer is put in place and the NFET can be implanted. Then a second spacer is put in place and the PFET is implanted. Since the PFET uses boron as an implant species, the boron diffuses much faster than arsenic during heat cycles, thus requires that the deep junction be placed further away from the gate than the arsenic deep junction, thus the need for multiple spacers. However, the subsequent cobalt silicide formation is limited by the distance of the final 2nd spacer, thus keeping this silicide at a distance of several hundred angstroms. The NFET has been shown to have the highest performance when the silicide is very much closer to the gate, so the double spacer technique does not produce the fastest NFET. If a single narrow spacer was used, the NFET would be optimized, but the close proximity of the silicide for the PFET, along with deep junction overrun will make a poor performance PFET.

Our technique descibes a method and structure where the first spacer is made and the NFET is implanted as mentioned above. Then a second spacer is formed and the PFET can be implanted. The optimized films for these spacers was a nitride film using an LTO oxide underlayer as the etch stop. Finally, after the second spacer is formed and implanted, a mask is used to block off the PFETS and cover them with photoresist. A dry nitride etch is then performed which selectively removes the silicon nitride second spacer, stopping selectively on the LTO etch stop. The photoresist is then removed, leaving a double nitride spacer on the PFETs and a single nitride spacer on the NFETs, giving the optimal spacer for each type of device. Futhermore, during silicide formation, the LTO etch stop film on the nitride will be removed by HF prior to silicide, leading to a silicide edge very close to the gates for the NFETs while the double nitride spacer on the PFETs prevents the silicide from getting too close th the gate, which

Improved Double Gate Device

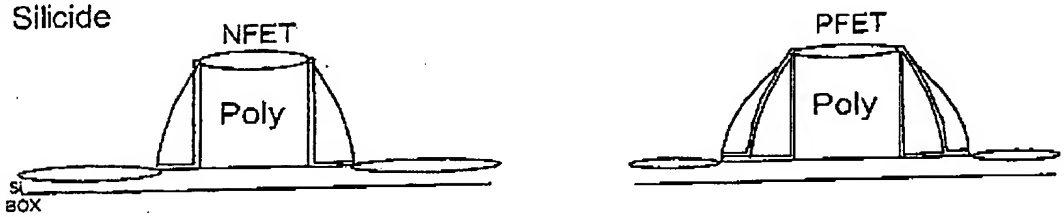


[redacted]

/D. Schepis/Sadanand Deshpande

Improved Double Gate Device

Wet etch LTO
Form Silicide



[redacted]

/D. Schepis/Sadanand Deshpande